AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1 and 35-38 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A liquid crystal display, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and crossing over said plurality of gate lines;

a plurality of pixel regions defined by the crossing of said plurality of gate lines and said plurality of data lines;

a semiconductor layer comprising a semiconductor pattern and a light interception pattern;

a common electrode formed in each pixel region;

a pixel electrode formed in each pixel region, spaced apart from said common electrode with a predetermined distance therebetween; and

a thin film transistor provided to each pixel region and including ~~a~~ the semiconductor pattern~~; and~~

~~a light interception pattern formed of the same layer as the semiconductor pattern~~.

2. (Previously Presented) The liquid crystal display of claim 1, wherein said light interception pattern and said data line corresponding thereto overlap each other, and said light

interception pattern and said common electrode or said pixel electrode close to said data line corresponding thereto overlap each other.

3. (Previously Presented) The liquid crystal display of claim 1, wherein said light interception pattern and a common electrode or a pixel electrode of a neighboring pixel region overlap each other.

4. (Previously Presented) The liquid crystal display of claim 1, wherein the semiconductor pattern is connected to said light interception pattern corresponding thereto.

5. (Previously Presented) The liquid crystal display of claim 1, wherein the semiconductor pattern is extended to said data line corresponding thereto.

6. (Previously Presented) The liquid crystal display of claim 1, wherein the light interception pattern is extended beyond a periphery of said data line corresponding thereto.

7. (Previously Presented) The liquid crystal display of claim 1, wherein said common electrode is formed on the same plane as said plurality of gate lines.

8. (Previously Presented) The liquid crystal display of claim 1, wherein said pixel electrode is formed on the same plane as said plurality of data lines.

9. (Previously Presented) The liquid crystal display of claim 1, wherein said pixel electrode is formed on the plane different from said plurality of data lines.

10. (Previously Presented) A liquid crystal display, comprising:

an insulating substrate;

a gate line assembly formed on said substrate and comprising a plurality of gate lines, and a plurality of gate electrodes connected to the gate lines;

a common electrode formed on the substrate and separated from said gate line assembly;

a gate insulating layer covering said gate line assembly and said common electrode;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes;

a light interception pattern formed on the gate insulating layer and formed of the same material as said semiconductor pattern;

a data line assembly comprising:

a source electrode and a drain electrode formed on said semiconductor pattern, and

a plurality of data lines connected to the source electrode and crossing over said plurality of gate lines to define a pixel region; and

a pixel electrode formed in the pixel region and alternatively located side by side with the common electrode, wherein the pixel electrode is coupled to the drain electrode.

11. (Previously Presented) The liquid crystal display of claim 10, wherein said light interception pattern and the data line corresponding thereto overlap each other, and said light

interception pattern and the common electrode or the pixel electrode close to the data line corresponding thereto overlap each other.

12. (Previously Presented) The liquid crystal display of claim 10, wherein said light interception pattern and said common electrode or said pixel electrode of a neighboring pixel region overlap each other.

13. (Previously Presented) The liquid crystal display of claim 10, wherein said semiconductor pattern is connected to said light interception pattern corresponding thereto.

14. (Previously Presented) The liquid crystal display of claim 13, wherein the semiconductor pattern is extended to the data line corresponding thereto.

15. (Previously Presented) The liquid crystal display of claim 14, wherein said light interception pattern is extended beyond a periphery of the data line corresponding thereto.

16. (Previously Presented) The liquid crystal display of claim 14, wherein said semiconductor pattern has the same shape as the data line except for a channel portion between the source electrode and the drain electrode.

17. (Previously Presented) The liquid crystal display of claim 10, wherein said pixel electrode is formed on the same plane as the plurality of data lines.

18. (Previously Presented) The liquid crystal display of claim 17, wherein said semiconductor pattern is extended to said pixel electrode.

19. (Previously Presented) The liquid crystal display of claim 10, further comprising a protective layer covering said data line assembly and having a contact hole, wherein said pixel electrode is formed on the protective layer and connected to the drain electrode through the contact hole.

20. (Previously Presented) The liquid crystal display of claim 10, further comprising an ohmic contact pattern interposed between said semiconductor pattern and said data line assembly.

21. (Previously Presented) The liquid crystal display of claim 20, wherein the ohmic contact pattern has the same shape as the plurality of data lines.

22. (Previously Presented) A method for fabricating a liquid crystal display, comprising the steps of:

forming a gate line assembly and a common line assembly on an insulating substrate, the gate line assembly comprising gate lines and gate electrodes, and the common line assembly comprising common electrodes;

forming a gate insulating layer on the substrate covering the gate line assembly and the common line assembly;

forming a semiconductor pattern and a light interception pattern, both formed of the same material, on the gate insulating layer;

forming a data line assembly on the gate insulating layer, the data line assembly comprising a source electrode and drain electrode, and a plurality of data lines; and

forming a pixel electrode.

23. (Previously Presented) The method of claim 22, wherein the data line assembly is formed on the same plane as the pixel electrodes.

24. (Previously Presented) The method of claim 23, wherein the light interception pattern, the semiconductor pattern, the data line assembly and the pixel electrode are patterned by photoresist patterns.

25. (Previously Presented) The method of claim 24, wherein the photoresist patterns comprise:

a first pattern with a predetermined thickness placed at a channel portion between the source and the drain electrodes as well as at the light interception pattern,

a second pattern having a thickness larger than the thickness of the first pattern, and

a third pattern having a thickness smaller than the thickness of the first pattern.

26. (Previously Presented) The method of claim 25, wherein the photoresist patterns are formed by a single mask.

27. (Previously Presented) The method of claim 26, wherein said steps of forming the semiconductor pattern, the light interception pattern, the data line assembly and the pixel electrode, further comprise the steps of:

sequentially depositing a semiconductor layer and a conductive layer on the gate insulating layer;

coating a photoresist film onto the conductive layer;

exposing the photoresist film to light through the mask;

developing the photoresist film to form the photoresist patterns, the second photoresist pattern being placed over the data line assembly;

etching the conductive layer under the third photoresist pattern and the underlying semiconductor layer to form the semiconductor pattern and the light interception pattern;

removing the first photoresist pattern through ashing;

etching the conductive layer the second photoresist pattern as mask to complete the data line assembly and the pixel electrodes; and

removing the remaining photoresist pattern.

28. (Previously Presented) The method of claim 27, wherein the semiconductor pattern has the same shape as the data line assembly except for the channel portion between the source electrode and the drain electrode.

29. (Previously Presented) The method of claim 28, wherein the light interception pattern, the semiconductor pattern and the data line assembly are formed by a photoresist pattern.

30. (Previously Presented) The method of claim 29, wherein the photoresist pattern comprises:

a first pattern with a predetermined thickness placed at the channel portion between the source electrode and the drain electrode,

a second pattern having a thickness larger than the thickness of the first pattern, and

a third pattern having a thickness smaller than the thickness of the first pattern.

31. (Previously Presented) The method of claim 30, wherein the photoresist pattern is formed by a single mask.

32. (Previously Presented) The method of claim 31, wherein said step of forming the semiconductor pattern, the light interception pattern, and the data line assembly further comprises steps of:

sequentially depositing a semiconductor layer and a conductive layer on the gate insulating layer;

coating a photoresist film onto the conductive layer;

exposing the photoresist film to light through the mask;

developing the photoresist film to photoresist patterns, the second photoresist pattern being placed over the data line assembly;

etching the conductive layer under the third photoresist pattern and the underlying semiconductor layer to form the semiconductor patterns and the light interception patterns;

removing the first photoresist pattern through etch back, and etching the second photoresist pattern;

etching the conductive layer using the second photoresist pattern as mask to complete the data line assembly; and

removing the remaining photoresist pattern.

33. (Previously Presented) The method of claim 32, wherein the pixel electrode is formed on the plane different from the data line assembly.

34. (Previously Presented) The method of claim 33, further comprising the step of:

forming a protective layer after forming the data line assembly to cover the data line assembly; and

forming the pixel electrodes on the protective layer.

35. (Currently Amended) A liquid crystal display, comprising:

a gate line formed on a substrate;

a data line insulated from and intersecting said gate line;

a semiconductor layer comprising a semiconductor pattern and a light interception pattern;

a thin film transistor connected to said gate line and said data line, said thin film transistor including ~~a~~ the semiconductor ~~layer~~ pattern; and

a field-generating electrode having a portion laterally spaced apart from said data line with a gap therebetween~~; and~~,

wherein the light interception pattern overlaps the gap ~~a light interceptor made of the same layer as the semiconductor layer and overlapping the gap~~.

36. (Currently Amended) The liquid crystal display of claim 35, wherein said light ~~interceptor~~ interception pattern and said data line overlap each other, and said light ~~interceptor~~ interception pattern and said field-generating electrode overlap each other.

37. (Currently Amended) The liquid crystal display of claim 35, wherein the semiconductor layer is connected to said light ~~interceptor~~ interception pattern.

38. (Currently Amended) The liquid crystal display of claim 35, wherein said light ~~interceptor~~ interception pattern is wider than said data line.